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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,267	01/20/2004	Geum-Jin Yun	2557-000206/US	6863

30593 7590 05/22/2006

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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,267	YUN ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14 and 16-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-14 and 16-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "S15" in fig. 2A-B has been used to designate both "cooling" and "temperature control". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 8, 12 and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Horisaki et al. (JP 2001-155497).

Regarding claims 1 and 21, Horisaki et al. (hereafter Horisaki) in fig. 1 discloses an integrated burn-in test method for testing a multi-chip package, comprising:

uploading an integrated burn-in test program [from 2, see fig. 1] to the burn-in equipment [1 or 4] for testing the multi-chip package [3 of fig. 1 and last four lines of paragraph 0006 at page 6 of 14]; and

conducting a test of the multi-chip package using the integrated burn-in test program [using 2 and 3, see paragraphs 0009 and 0010 at pages 7-8 of 14]; wherein

the multiple kinds of semiconductor devices include at least one of non-volatile memory, a SRAM and a DRAM, and the integrated burn-in test program is adapted to test at least one of the non-volatile memory, the SRAM and the DRAM [lines 6-10 of paragraph 0009 at page 6 of 14].

Regarding claim 4, Horisaki discloses the multi-chip package performs a memory function [e.g. SRAM].

Regarding claims 8 and 22, Horisaki discloses the integrated burn-in test program uses a multiplexer selection function for applying a desired test condition [fig. 3 and paragraph 0005 and 0008] during testing of each semiconductor device.

Regarding claim 12, Horisaki discloses the burn-in test is a monitoring burn-in test [using screen].

3. Claims 1, 14, 16-17, 20-21, 27 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Tom et al. (MCM BURN-IN EXPERIENCE).

Regarding claims 1, 14 and 21, Tom et al. (hereafter Tom) in fig. 1 discloses uploading a burn-in test program, conducting contact test on each of the semiconductor devices [chips and section III], conducting sequentially [see fig. 1] a burn-in test [1st paragraph under section III] using test program [line 1 of section IV and stimulation, thermal control of section III] for each of the semiconductor devices and program controls the chamber temperature [section III and "Thermal Control" section of page 226, particularly 1st line of 3rd paragraph], ending the test and bin shorting [see fig. 1], as further claimed.

Regarding claim 16, Tom discloses memory [CMOS].

Regarding claims 17 and 27, Tom discloses program for masking and blocking as further claimed using BIST and setting different temperature condition for each of the semiconductor devices [line 1 of 4th paragraph under "Thermal Control" section at page 226].

Regarding claim 20, Tom discloses monitoring burn-in test [see section "Thermal Control" at page 226].

Regarding claim 29, Tom discloses the burn-in board [the module substrate of section II] and a chamber ["module burn-in" of section III] of the burn-in equipment ["test equipment" of section III] as further claimed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-7, 9-11, 13, 19, 23-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horisaki as applied to claims 1, 14 and 21 above, and further in view of Applicant admitted prior art (fig. 2A-2B) and Eide (US 6014316)

Regarding claims 5 and 24, Horisaki discloses all the elements, except for the test is conducted for each semiconductor device of the multi-chip package at a different temperature or specific temperature. However, Applicant admitted prior art (hereafter APA) at fig. 2A-2B discloses the test is conducted for each semiconductor device of the multi-chip package at a different temperature or a specific temperature. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Horisaki with testing each semiconductor device of the

multi-chip package at a different temperature as taught by APA, in order to do burn-in test on each semiconductor device.

Regarding claim 6, APA discloses a burn-in board and the chamber of burn-in equipment, as further claimed at paragraph 0008.

Regarding claim 7, Horisaki and APA is silent about the multi-chip package is in the form of a TBGA (thin ball grid array). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use TBGA, since it was known in the art that TBGA package also contains plurality of IC's or semiconductor devices for testing and packaging. Eide at fig. 7 and at lines 16-39 discloses TBGA to provide dense electronic package.

Regarding claims 9 and 23, Horisaki is silent about the integrated burn-in test program has an I/O masking function for blocking some I/O terminals. Rather, at lines 7-10 of paragraph 0010, Horisaki discloses selection of number of I/O of semiconductor memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use test program as claimed to block I/O terminals, since test program with masking function as claimed is well known in the art for control application, particularly in code development program using address line.

Regarding claim 10, Horisaki discloses all the elements except for the integrated burn-in test program has a function of setting a burn-in temperature condition for different kinds of semiconductor devices. APA discloses the integrated burn-in test program has a function of setting a burn-in temperature condition for different kinds of semiconductor devices. Therefore, it would have been obvious to one having ordinary

skill in the art at the time the invention was made to modify Horisaki to include test program as taught by APA for burn-in testing the semiconductor devices.

Regarding claims 11 and 25, APA discloses after loading the multi-chip package on the burn-in board to the chamber of the burn-in equipment, a contact test [step 11] is conducted to examine whether an electrical connection of the burn-in board is correct.

Regarding claims 13 and 26, Horisaki is silent about the integrated burn-in test program requires only one time bin sorting based on the burn-in test result. APA discloses one time bean sorting. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made modify the program pf Horisaki to include sorting as taught by APA, in order to sort the defective component from the good component.

Regarding claim 19, Tom is silent about the multi-chip package is in the form of a TBGA (thin ball grid array). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use TBGA, since it was known in the art that TBGA package also contains plurality of IC's or semiconductor devices for testing and packaging. Eide at fig. 7 and at lines 16-39 discloses TBGA to provide dense electronic package.

Regarding claim 28, Horisaki is silent about a chamber as further claimed. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a chamber, since it was known in the art that use of chamber during testing for the purpose of control and safety. APA also discloses a chamber for its testing of multi-chip module during testing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paresh Patel 05/11/06
Paresh Patel
Primary Examiner
Art Unit 2829

May 11, 2006